Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of arbitrating ~~carrying out arbitration~~ in a packet exchanger that includes ~~including an~~ input ~~buffer~~ buffers temporarily storing ~~a packet~~ packets ~~having arrived at an input port~~, and a packet switch which switches ~~a packet~~ packets between ~~a specific~~ input ~~port~~ ports and ~~a specific~~ output ports ~~port~~, said method comprising ~~the steps of~~:

receiving a first plurality of sequences, each of the first plurality of sequences including cells that make up a packet;

[[(a)]] concurrently processing the ~~carrying out a~~ first plurality of sequences to select output ports to correspond to the input ports, the selections being made among output ports that have not been selected to correspond to an input port ~~in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order~~; and

~~(b) making an allowance~~ assigning the packet in each of said first plurality of sequences ~~for packets~~ to be output through the output ports at different times from one another.

2. (canceled)

3. (canceled)

4. (currently amended) The method as set forth in claim 1, wherein said processing the first plurality of sequences ~~basic process~~ is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet, and wherein said ~~basic process being~~ processing is carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

5. (currently amended) The method as set forth in claim 1, further comprising ~~the step of~~ concurrently processing ~~carrying out~~ a second plurality of sequences after said first plurality of sequences have been processed ~~carried out~~.

6. (currently amended) The method as set forth in claim 5, wherein said second plurality of sequences is ~~carried out~~ processed in an order ~~just~~ opposite to an order in which said first plurality of sequences is processed ~~carried out~~.

7. (currently amended) The method as set forth in claim 5, wherein said first plurality of sequences starts being ~~carried out~~ processed at a first time and said second plurality of sequences starts being ~~carried out~~ processed at a

second time later than said first time ~~by a predetermined period of time~~.

8. (currently amended) The method as set forth in claim [[3]] 1, wherein processing the first plurality of sequences further includes ~~each of said basic processes includes the steps of~~:

(a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers; and

(b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers.

9. (currently amended) The method as set forth in claim 8, wherein said ~~step~~ (a) is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet, and said ~~step~~ (b) is completed in a half of said unit period of time.

10. (currently amended) The method as set forth in claim [[2]] 1, further comprising ~~wherein said step (c) includes the steps of~~:

(c1) carrying out said ~~basic processes~~ processing for all of said input buffers with respect to a packet having a higher priority; and

(c2) carrying out said ~~basic processes~~ processing for all of said input buffers with respect to a packet having a lower priority.

11. (currently amended) The method as set forth in claim 10, wherein

~~each of~~ said processing ~~basic processes~~ is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

12. (currently amended) The method as set forth in claim 10, wherein ~~each of~~ said processing ~~basic processes~~ is completed in a unit ~~of~~ period of time defined as a period of time necessary for said input buffers to output a packet, and wherein another sequence starts being carried out after said ~~step~~ (c1) ~~have~~ has been completed.

13. (original) The method as set forth in claim 1, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

14. (currently amended) An arbiter circuit ~~constituting~~ for arbitrating for a packet exchanger comprising:

~~together with an~~ input ~~buffer~~ buffers for temporarily storing ~~a packet~~ packets having arrived at ~~an~~ input ~~port~~ ports;

~~, and~~ a packet switch which switches a packet between a specific input port and a specific output port, said arbiter circuit configured to ~~having functions of~~:

(a) concurrently process ~~carrying out~~ a first plurality of sequences, each said sequences including cells that make up a packet, to select output ports that have not been selected to correspond to the input ports, the selections being

made among output ports that are not currently selected to correspond to an input port ~~in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order~~; and

(b) ~~making an allowance~~ assign the packet in each of said first plurality of sequences ~~for packets to be~~ for output through the output ports at different times from one another.

15. (canceled)

16. (canceled)

17. (currently amended) The arbiter circuit as set forth in claim 14, wherein said concurrently processing the first plurality of sequences ~~basic process~~ is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet, and wherein said ~~basic process being~~ concurrently processing is carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

18. (currently amended) The arbiter circuit as set forth in claim 14, wherein said arbiter circuit ~~further includes a function of~~ concurrently processes ~~carrying out~~ a second plurality of sequences after ~~carrying out~~ processing said first plurality of sequences.

19. (currently amended) The arbiter circuit as set forth in claim 18, wherein said arbiter circuit ~~carries out~~ processes said second plurality of sequences in an order ~~just~~ opposite to an order in which said arbiter circuit ~~carries out~~ processes said first plurality of sequences.

20. (currently amended) The arbiter circuit as set forth in claim 18, wherein said arbiter circuit starts ~~carrying out~~ processing said first plurality of sequences at a first time and said second plurality of sequences at a second time later than said first time ~~by a predetermined period of time~~.

21. (currently amended) The arbiter circuit as set forth in claim [[16]] 14, wherein said arbiter circuit selects an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers, and then selects an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers~~, in each of said basic processes~~.

22. (original) The arbiter circuit as set forth in claim 21, wherein said arbiter circuit selects said input buffer in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

23. (currently amended) The arbiter circuit as set forth in claim [[15]]

14, wherein said arbiter circuit ~~carries out~~ performs said ~~basic processes~~ processing for all of said input buffers ~~firstly with respect to a packet~~ having a higher priority packet before processing input buffers, and secondly with respect to a packet having a lower priority.

24. (currently amended) The arbiter circuit as set forth in claim 23, wherein said arbiter circuit carries out ~~each of~~ said ~~basic processes~~ processing in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet.

25. (currently amended) The arbiter circuit as set forth in claim 23, wherein said arbiter circuit carries out ~~each of~~ said ~~basic processes~~ processing in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and starts ~~carrying out~~ processing another sequence after said processing of the first plurality of sequences ~~basic processes have been completed~~.

26. (currently amended) The arbiter circuit as set forth in claim 14, wherein said arbiter circuit further includes:

(a) a plurality of unit modules each associated with at least one of said input ~~buffer~~ buffers and said output ports ~~port~~, each of said unit modules processing the first plurality of sequences ~~carrying out said basic processes~~; and

(b) a signal line connecting said unit modules to one another in a ring.

27. (currently amended) The arbiter circuit as set forth in claim 14, wherein said arbiter circuit further includes:

(a) a plurality of unit modules each associated with at least one of said input ~~buffer~~ buffers and said output ports ~~port~~, each of said unit modules carrying out processing of the first plurality of sequences ~~said basic processes~~;

(b) a first signal line connecting said unit modules to one another in a ring, a signal being transmitted through said first signal line in a first direction; and

(c) a second signal line connecting said unit modules to one another in a ring, a signal being transmitted through said second signal line in a second direction opposite to said first direction.

28. (currently amended) The arbiter circuit as set forth in claim 14, wherein said arbiter circuit includes:

(a) a plurality of unit modules each associated with at least one of said input ~~buffer~~ buffers and said output ports ~~port~~, each of said unit modules carrying out processing of the first plurality of sequences ~~said basic processes~~;

(b) a first signal line connecting said unit modules to one another in a ring, a higher priority signal ~~having a higher priority~~ being transmitted through said first signal line; and

(c) a second signal line connecting said unit modules to one another in a ring, a lower priority signal ~~having a lower priority~~ being transmitted through said

second signal line.

29. (original) The arbiter circuit as set forth in claim 14, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

30. (currently amended) A recording medium readable by a computing device ~~computer,~~ and storing a program therein for causing ~~a computer~~ the computing device to carry out a method of arbitrating ~~carrying out arbitration~~ in a packet exchanger that includes ~~including an~~ input ~~buffer~~ buffers temporarily storing ~~a packet~~ packets ~~having arrived at an input port~~, and a packet switch which switches ~~a packet~~ packets between ~~a specific~~ input ~~port~~ ports and ~~a specific~~ output ports ~~port~~, said method comprising ~~the steps of~~:

[[(a)]] concurrently processing ~~carrying out~~ a first plurality of sequences, each said sequence including cells that make up a packet, to select output ports, the selections being made among output ports that do not correspond to an input port ~~in each of said sequences basic processes for at least one of said input buffer and said output port are carried out in a predetermined order~~; and

[[(b)]] ~~making an allowance~~ assigning the packets in each of said first plurality of sequences ~~for packets to be~~ for output through the output ports at different times from one another.

31. (canceled)

32. (canceled)

33. (currently amended) The recording medium as set forth in claim 30, wherein said processing the first plurality of sequences ~~basic process~~ is completed in a unit period of time defined as a period of time necessary for said input buffers to output a packet, and wherein said ~~basic process being~~ processing is carried out for at least one of said input buffers and said output ports in each of said sequences in said unit period of time.

34. (currently amended) The recording medium as set forth in claim 30, wherein said method further includes ~~the step of~~ concurrently ~~carrying out~~ processing a second plurality of sequences after said first plurality of sequences ~~have been carried out~~.

35. (currently amended) The recording medium as set forth in claim 34, wherein said second plurality of sequences is processed ~~carried out~~ in an order ~~just~~ opposite to an order in which said first plurality of sequences is processed ~~carried out~~.

36. (currently amended) The recording medium as set forth in claim 34, wherein said first plurality of sequences starts being carried out at a first time and said second plurality of sequences starts being carried out at a second time

later than said first time ~~by a predetermined period of time~~.

37. (currently amended) The recording medium as set forth in claim 30, wherein ~~each of~~ said ~~basic processes~~ processing includes ~~the steps of~~:

(a) selecting an input buffer to be allowed to output a packet having a higher priority among packets accumulated in said input buffers; and

(b) selecting an input buffer to be allowed to output a packet having a lower priority among packets accumulated in said input buffers.

38. (currently amended) The recording medium as set forth in claim 37, wherein said ~~step~~ (a) is completed in a half of a unit period of time defined as a period of time necessary for said input buffers to output a packet, and said ~~step~~ (b) is completed in a half of said unit period of time.

39. (currently amended) The recording medium as set forth in claim [[31]] 30, further including ~~wherein said step (c) includes the steps of~~:

(c1) carrying out said ~~basic processes~~ processing for all of said input buffers with respect to a packet having a higher priority; and

(c2) carrying out said ~~basic processes~~ processing for all of said input buffers with respect to a packet having a lower priority.

40. (currently amended) The recording medium as set forth in claim 39, wherein ~~each of~~ said ~~basic processes~~ processing is completed in a half of a

unit period of time defined as a period of time necessary for said input buffers to output a packet.

41. (currently amended) The recording medium as set forth in claim 39, wherein ~~each of~~ said ~~basic processes~~ processing is completed in a unit of period of time defined as a period of time necessary for said input buffers to output a packet, and wherein another sequence starts being carried out after ~~said step~~ (c1) ~~have~~ has been completed.

42. (original) The recording medium as set forth in claim 30, wherein the number of said sequences is equal to the number of ports in said packet exchanger.

Claims 43-58 (canceled)